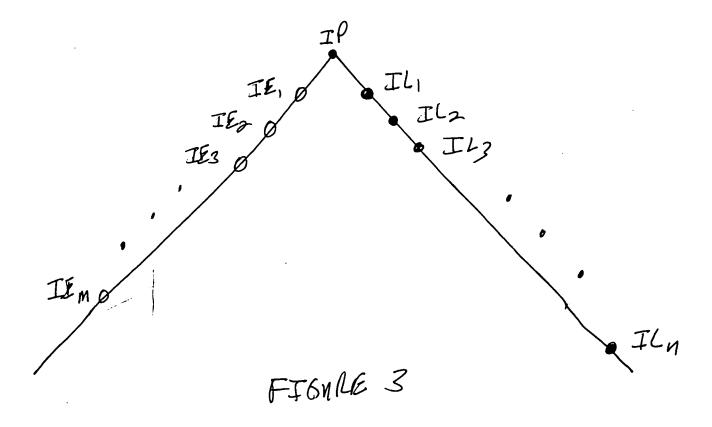


FIGURE 1



V 10 FIGURE 2 16 12-EM Received Signal JEM 14-Em 12-E3 IE3 - 14-E3 PROCESSOR 12-E2 IE2 FAULT 14-E2 -12-E1 IEI 14-E1 12-1 IP 12-61 エムし 12-L2 -12-L3 ILB TLn 14-Ln-